Study of on-die EMI model for Center-placed PAD DRAM

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Abstract

Generally, bondwire is main radiation point at chip level emi. Recently, EMI radiation is seen in the DIE region of the LPDDR5 center-placed pad DRAM. While changing the DIE RDL structure, EMI simulation was performed using SIwave to determine the cause of EMI radiation. By dividing into an ideal structure and a structure that increases radiation, it is possible to identify the cause of EMI occurrence and effectively simulate EMI. It was confirmed that EMI radiation by the center-placed pad occurs when the current flowing through the power and VSS is disturbed by the slit/slot. Using this, it is possible to perform a more sophisticated EMI simulation

1 Introduction

Various wireless devices are increasing. Accordingly, the importance of EMI in ICs is increasing. So far, in many cases, the die part is not assumed to be the main factor. In particular, in case of using stack die, bondwire was considered as the main radiating element. However, it was confirmed that radiation from DIE occurred significantly. [1] Near field simulation by modeling the entire die cannot proceed due to the complexity of the silicon die. As an alternative, the EMI DIE model using floating metal [2] was used, but this part has the following disadvantages. The actual power layout is not a plane. It is made like a fish bone to supply current to the circuit block. RDL trace are connected to top metal through RDL VIA. Therefore, in this paper, we discuss the effective die model method.

2 Method

We want to predict the DRAM EMI level from the package design file and the IC layout design file. For this, the PKG file is used as it is and a simplified DIE model is required.

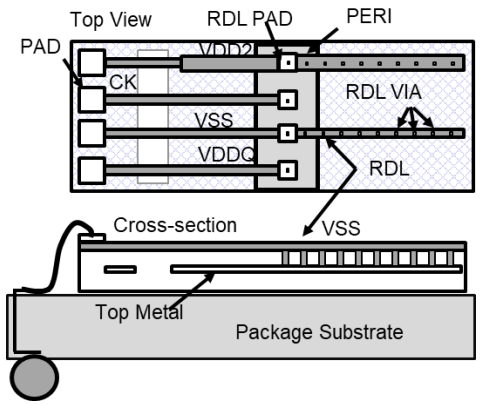

Figure 1: DIE including RDL and Top Metal

As shown in Figure 1, a long loop is formed in the center-placed pad layout architecture. And, there is a power plane under the RDL. In the case of DRAM, the number of layers is small for low cost implementation, and the top metal under RDL is not an ideal plane. That is, VSS, Power, and Buses are mixed. When the circuit blocks are placed, in reality, it is not easy to implement the ideal power plane without slit or slot. In addition, various types of power such as VDD2H and VDD1 are used. Also, the number of PADs allocated to each power cannot be used arbitrarily, so in most cases it cannot be made symmetrical

2.1 Simplified Model

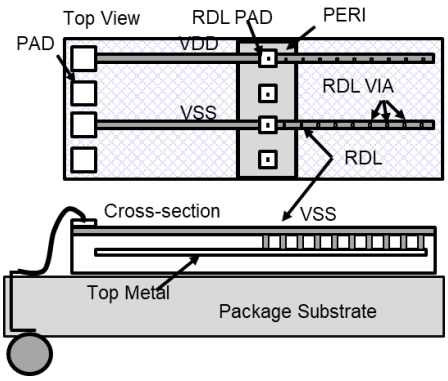

Figure 2: Typical die layout architecture

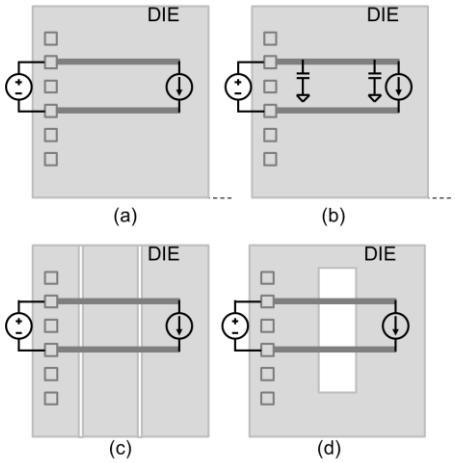

Figure 3: Simple structure model causing EMI

Figure 2 shows the extracted structure shown in Figure 1 in the case of typical die layout architecture. Figure 3 shows a simple structure model including EMI: (a) basic simple model (b) floating metal model + cap model (c) slit floating metal model (d) slot model

3 Results

Through the Simple Structure Model, it was confirmed that Figure 3 (d) is the largest factor. That is, it could be confirmed that the effect by the slot was the largest. Based on the SIwave results for a simple model, a model for the real structure was carried out. We would like to share the simulation results for LPDDR5 products as shown in Table 1 at the conference.

Model Case	Note
PKG (only)	
PKG+RDL	
PKG+RDL+Chip Metal	Floating metal
PKG+RDL+Modifed Metal	Proposed Model

Table 1: EMI Simulation Case

4 Discussion

EMI SIM, including the entire silicon DIE, is structurally too complex to conduct EMI simulation. Therefore, in order to estimate the amount of EMI radiation from the DRAM chip, the PKG-only SIM can proceed. For more accurate EMI simulation, it is necessary to simulate including the effect of DIE. To realize this, in this paper, the structurally ideal RDL structure and the structure causing EMI radiation were analysed separately. Through this method, it is expected that the cause of the issue can be accurately explained and optimized efficiently.

Acknowledgements

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References

[1] J.-B. Kim *et al.*, “A Low EMI characteristic of LPDDR5 SDRAM with Edge-placed PADs and Short Re-Distribution Lines,” in *2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, Aug. 2022, pp. 64–68. doi: 10.1109/EMCSI39492.2022.9889642.

[2] J.S. Youn *et al*., “Chip and Package-Level Wideband Analysis for Mobile DRAM Devices EMI” Proc. DesignCon 2016. .